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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., AND AEROFLEX COLORADO SPRINGS, INC.

Defendants.

SYNOPSYS, INC.,

Plaintiff,

vs.

RICOH COMPANY, LTD.,

Defendant.

Case No. C03-04669 MJJ (EMC)

Case No. C03-02289 MJJ (EMC)

OPPOSITION TO RICOH'S LOCAL RULE 6-3 MOTION TO ENLARGE TIME REGARDING THE MOTION FOR RULE 11 SANCTIONS

Ricoh's motion to extend time should be denied. Ricoh has had more than ample time to respond to Defendants' ripe Motion for Rule 11 sanctions.[1] Ricoh's argument that its trial preparation should trump what is a very serious and ripe dispute that may itself moot the need for a trial is not well taken. Rather than dismiss this case or appeal or seek clarification of the Court's Claim Construction Order, Ricoh and its counsel have dragged Defendants through a year of extremely expensive and burdensome litigation, demanded the production of 12 million pages of documents, filed numerous motions, and taken more than 240 hours of depositions, only for Defendants to discover that counsel's sole theory of infringement in this one patent, one independent claim, literal infringement case is one that has already been rejected by this Court. Ricoh's motion to extend time demonstrates that Ricoh has no non-frivolous substantive response to Defendants' Rule 11 Motion. The time for Ricoh and its counsel to respond to this Motion is now, not after many more months of additional party and judicial resources are wasted.

The Rule 11 Motion is based on counsel's continued assertion in signed pleadings that Defendants infringe the '432 patent. *See* Case 03-4669 Docket No. 664 (Rule 11 Motion) at 11:18-26. Rule 11 sanctions are appropriate because Ricoh's and its counsel's continued assertion of infringement is premised on an infringement theory that Ricoh and its counsel know contradicts the Court's Claim Construction Order. Ricoh argues that the Rule 11 Motion is procedurally flawed and should be postponed indefinitely because counsel cannot be sanctioned for relying on the "inadequate opinions and conclusions of its experts." Ricoh, however, cannot hide behind its expert. Ricoh's and its counsel's instructions to its expert and reliance on its expert are not objectively reasonable. Instead of relying on its current expert witness on infringement Ricoh's counsel hired a special expert to opine on a single infringement issue, which as explained in the Rule 11 Motion, evidences a consciousness of guilt. *See* Rule 11 Motion at 4-5; 10-11. Moreover, counsel instructed the specially hired expert on what to do. It is Ricoh's and Ricoh's counsel's instructions to its specially hired expert as well as its

[1] The Rule 11 Motion was served on Ricoh on August 19, 2006. Ricoh's opposition is due on September 26. Thus, Ricoh will have had five weeks to respond to the Motion. Moreover, that the Rule 11 Motion relies on facts that are the basis of a pending summary judgment motion is irrelevant. Certainly, the same Rule 11 motion could have been filed without filing the summary judgment motion, and thus, it is not premised on the summary judgment motion being granted.

continued assertion of infringement in various pleadings, including Ricoh's opposition to Defendants' Motion for Summary Judgment of Noninfringement Number 1 (RTL), signed by counsel and filed with the Court that give rise to the Rule 11 Motion. *Coffey v. Healthtrust, Inc.*, 1 F.3d 1101, 1004 (10th Cir. 1993) (reliance on expert opinion must be reasonable).

The issue presented in the Rule 11 Motion is whether Ricoh has a good faith basis to assert that the Defendants infringe the patent. Specifically, the question is whether this is a good faith basis for the Ricoh's assertion that the Customer Defendant inputs fall outside the scope of the inputs specifically disclaimed by the patentee during patent prosecution. The Court has already and quite clearly determined the scope of the disclaimer in its Claim Construction Order. To determine the scope of the disclaimer, the Court examined the prosecution history and the teachings of the Darringer patent "to examine how closely it reads on" the '432 patent. Exhibit 1 (Claim Construction Order ("CC Order") at 12:4-5). The Court determined that based on the teachings of the Darringer patent and the public record for the '432 patent that:

(1) Darringer included an explicit definition of RTL[2] that "the subsequent translation or transformation steps in [the Darringer patent] do not alter." Exhibit 1 (CC Order at 12:5-7).

(2) "The '432's public record fails to provide any support for Ricoh's distinction between 'structural' and 'functional' RTL-type input systems." Exhibit 1 (CC Order at 12:9-12).

(3) "[T]he prosecution history indicates that *the patentee disclaimed all register-transfer level descriptions*." Exhibit 1 (CC Order at 12:14-15) (emphasis added).

Accordingly, the Court construed "architecture independent actions and conditions" to exclude RTL as taught in Darringer.

Notwithstanding the clarity of the Court's order, Ricoh did not dismiss its case, seek reconsideration, or appeal the Court's order. Instead, Ricoh and its counsel hired an expert who is completely unfamiliar with the requirements of Design Compiler to testify solely on the issue of

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[2] As set forth in Defendants' Summary Judgment Motion 1 (Docket No. 568), an RTL description was explicitly defined as including a specification of inputs, outputs, latches (registers), and as well as, for each clock cycle, how the values of the outputs and latches (registers) are set based on the values of the inputs and previous values of the latches (registers). Ricoh's expert report does not address this issue. *See* Exhibit 3 at 13-16.

"architecture independent actions and conditions."[3] Ricoh's counsel then instructed that expert to examine teachings of the Darringer patent and the public record to determine the meaning of "RTL as taught in Darringer," even though the Court already fully considered and ruled on the teachings of Darringer as well as the scope of the disclaimer and concluded that the patentee disclaimed all register-transfer level descriptions.[4] Counsel did not ask the specially hired expert *to form an opinion about whether or not the inputs were register-transfer level description.*[5] Indeed, Dr. Papaefthymiou testified that if the Court already examined the teachings of Darringer and determined that the disclaimer excluded all register-transfer level descriptions "It's a completely separate question" than what is addressed in his report. Exhibit 2 at 124:18-125:3. Put simply, because of Ricoh's counsel's instructions and the premise of Dr. Papaefthymiou's expert report, Ricoh and its counsel are deliberately proceeding in this litigation without any basis for the contention that the Defendant inputs fall outside of the scope of the subject matter expressly disclaimed by the patentee.[6]

Indeed, Ricoh's specially hired expert based his opinions that the Customer Defendant inputs (of which he was never provided copies but only viewed small, counsel-selected segments of a handful of the 350+ designs at issue on WebEx calls – *see* Exhibit 2 at 66:17-22; 68:2-7; 191:13-192:20;

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[3] On August 11, 2006, Dr. Papaefthymiou testified he has never used Design Compiler; has no idea what inputs Design Compiler required; had not seen a single Customer Defendant design 11 days prior to his deposition; had never seen the HDL Operators Search Report that formed the basis for his opinion that evidenced all the actions and conditions; had never "read" any of the Customer Defendant depositions; admits that he has no opinion if the Court intended to exclude all RTL; and concedes that his methodology does not even work if applied to the relevant inquiry. Exhibit 2 at 18:23-19:5, 66:17-22, 75:6-24; 99:22-100:15, 124:18-125:3, 171:14-172:3, 175:8-22; 180:23-181:15.

[4] Exhibit 3 (Report at 2:15:18 ("This report also sets forth my opinion that these architecture independent inputs are not the type of "Register-Transfer Level (RTL)" formatted inputs specifications taught by the Darringer Patent (U.S. Patent No. 4,703,435) that was considered by the Court during claim construction); Exhibit 2 at 126:5-127:8 ("I have offered an opinion *independently of the court construction* about the nature of the inputs of the systems that the Darringer patent describes . . . ") (emphasis added).

[5] Dr. Papaefthymiou also testified that he "wasn't asked to look into the specific issue raised" on page 12, lines 9-12 as set forth in point (2) above. Exhibit 2 at 118:10-21. Dr. Papaefthymiou confirmed that he did not offer an opinion on whether the inputs were function or structural RTL or RTL at all. *Id*. at 44:4-22. And, Dr. Papaefthymiou acknowledges that of the exclusion of all RTL in the Court's claim construction order is inconsistent with his opinion: "You did point out something which may be viewed as an inconsistency on line 15. But, again, there needs to be a basis, and that basis is what you see between 16 and 19, between line 16 and 19. That was the basis for the report." *Id.* at 126:5-16.

[6] Ricoh's technical expert on all issues other than "architecture independent actions and conditions" agrees with Defendants, and as a long-time ASIC designer and user of Design Compiler, fully understands that the Defendants inputs are RTL. *See* Rule 11 Motion at 4-5; 10-11.16-17.

Exhibit 3 at Appendix B (list of materials considered)) are not "RTL as taught in Darringer" because his reading of the Darringer patent is that:

(1) "[T]he Darringer Patent uses the term *'RTL' in the sense of the older (then-prevalent) structural RTL. . .*" Exhibit 3 (Report at 13:6-8); and

(2) "[T]he requirement in the Darringer Patent that *the inputs undergo a simple translatio*n of the specification into equivalent AND/OR logic." Exhibit 3 (Report at 13:19-14:1; 15:7-9).

However, as described above on page 2, lines 13 through 20, the Court already considered the Darringer patent and the public record and expressly rejected both of these theories, concluding instead that the patentee disclaimed all RTL. Exhibit 1 (CC Order at 11-12). Because Ricoh's counsel did not ask its expert to consider this question, Ricoh and its counsel have no good faith basis for continuing with this suit, notwithstanding Ricoh's substantial efforts to create confusion here, in their opposition to Defendants' motion for summary judgment, and no doubt, in their to-be-filed opposition to Defendant's Rule 11 Motion.

Because Ricoh has no objective good faith basis on which to proceed, it wants to delay consideration of this motion indefinitely. The Court should reject this request. Defendants' Rule 11 Motion is not procedurally flawed. Moreover, it is not brought for an improper purpose, but rather for the salutary purpose of ending this litigation and recovering the costs of defending this case after the Court's Claim Construction Order. It is a procedurally and substantively proper motion that addresses very serious issues of misconduct on the part of Ricoh and/or its counsel, and seeks to avoid significant additional wasted resources (such as trial or trial preparation). If Ricoh or its counsel sought to have the Court's Claim Construction Order reconsidered, clarified[7] or evaluated on appeal, it should have taken steps to do so. It is both professionally irresponsible and sanctionable conduct to proceed with

[7] Read in the light most favorable to Ricoh and its counsel, Dr. Papaefthymiou's opinion is a further claim construction of the Court's Claim Construction Order, or more concisely, an expert opinion on claim construction. During claim construction, however, Ricoh argued vociferously that the Court should not consider expert testimony in interpreting the '432 claims. Docket No. 236 at 2:5-17, 8:12-20. Thus, even under this most favorable reading of Ricoh's position, Rule 11 sanctions are appropriate Ricoh's reliance on expert opinion regarding claim construction as its sole basis for continuing this suit is entirely contrary to the position it successfully advocated earlier in these proceedings. *See Helfand v. Gerson*, 105 F.3d 530, 534 (9th Cir. 1997) ("Judicial estoppel . . .precludes a party from gaining an advantage by taking one position, and then seeking a second advantage by taking an incompatible position.").

this litigation in view of the fact that the only basis on which Ricoh can maintain this litigation was to instruct a specially hired expert to provide an opinion that ignores, is contrary to, or reconsiders without leave, the Court's Claim Construction Order.

Despite Ricoh's argument, a response to the Rule 11 Motion would not require delving into attorney-client privileged or work product information of Ricoh and its counsel. Instead, the inquiry is solely an objective one: Did Ricoh and its counsel have an objectively reasonable basis on which to proceed? Whether Ricoh's and its counsel's decision to proceed was made in good or bad faith or due to incompetence is irrelevant. *See Cabell v. Petty*, 810 F.2d 463, 466 (4th Cir. 1987) ("Rule 11 does not prohibit merely intentional misconduct"); *see also Smith v. Ricks*, 31 F.3d 1478, 1488 (9th Cir. 1994 ("Counsel can no longer avoid the sting of Rule 11 sanctions by operating under the guise of a pure heart and an empty head.").

The seriousness of the issues here outweighs any alleged prejudice to Ricoh, including the need to move some alleged meetings whose nature remains undisclosed. Rather than push these issues out indefinitely, it is much more appropriate in view of all the resources that have already been wasted to date to have the Rule 11 Motion considered as quickly as possible. Notably, the parties do not need a ruling from the Court on summary judgment to determine how to respond to the Rule 11 Motion. Ricoh and its counsel can and should explain now, before a ruling on summary judgment, how its actions were objectively reasonable – if they are able to do so.

For all of these reasons, Defendants request that the Court deny Ricoh's Motion to Enlarge Time.

Dated: September 19, 2006

Respectfully submitted,

HOWREY LLP

By: */s/Denise M. De Mory*
Denise M. De Mory
Attorney for Defendants

FILED

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RICHARD W. WIEKING
CLERK, U.S. DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA

United States District Court
For the Northern District of California

IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SYNOPSYS, INC.,

Plaintiff,

v.

RICOH CO., LTD.,

Defendant.
_____/

RICOH CO., LTD.,

Plaintiff,

v.

AEROFLEX, INC., ET AL.,

Defendants.
_____/

No. C 03-2289 MJJ
No. C 03-4669

CLAIM CONSTRUCTION ORDER

INTRODUCTION

Before the Court is the parties' proposed construction of disputed terms contained in Plaintiff Ricoh Company, Ltd.'s ("Ricoh") patent. The suit involves an invention directed to a process for the design of application specific integrated circuits ("ASICs").

United States District Court
For the Northern District of California

FACTUAL BACKGROUND

This case concerns the alleged infringement of U.S. Patent Number 4,922,432 ("the '432 patent") entitled "Knowledge Based Method and Apparatus for Designing Integrated Circuits Using Functional Specifications." The issue before the Court is the construction of ten disputed terms contained in the patent.

The '432 patent, owned by Ricoh, claims methods for using a CAD design system to design an ASIC. "An [ASIC] is an integrated circuit chip designed to perform a specific function, as distinguished from standard, general purpose integrated circuit chips, such as microprocessors, memory chips, etc." '432 patent, col. 1:13-17. According to the '432 patent, the ASIC design processes of prior art require the designer to consider the required objectives and tasks of the desired ASIC and define the structural level design specification for that ASIC. This structural level design specification must define the various hardware components and their required interconnections, as well as a system controller for synchronizing the operations of those hardware components. This process requires an ASIC designer to have an "extensive and all encompassing knowledge" of these hardware components and their required interconnections. '432 patent, col. 1:28-31. There are only a small number of very large scale integration technology (VLSI) designers who possess the highly specialized skills needed to create structural level integrated circuit hardware descriptions.

The stated goal of the '432 patent's claimed invention is to enable the non-expert designer to design ASICs. The '432 patent claims a method for enabling the use of higher level input descriptions by allowing designers to describe ASIC specifications at a functional level. This functional level description is done without specification of structure, implementing technology, or architecture. This process involves taking architecture independent specifications and selecting previously designed circuit components or structure used as building blocks for implementing an ASIC. The process selects the optimum hardware cells to be included in the desired ASIC. Following this method, a user who does not have expertise in VLSI design can write architecture independent ASIC descriptions that ultimately can result in the automatic selection of hardware cells to be used in the ASIC.

Claim 13 of the '432 Patent is at issue in this proceeding. Independent claim 13 describes a

United States District Court
For the Northern District of California

process in which a designer describes an ASIC through an input specification using architecture independent descriptions. These architecture independent descriptions are used to select architecture dependent hardware cells. This process uses a library of definitions of the architecture independent, functional descriptions, a library of available hardware cells, and a expert system knowledge base. The expert system knowledge base contains a set of "rules" that embody the knowledge of VLSI experts. In order for each desired function to be performed by the ASIC, one of the definitions from the library of definitions is specified. The rules in the knowledge base are then applied to select architecture dependent hardware cells from the library of available hardware cells.

LEGAL STANDARD

The construction of a patent claim is a matter of law for the Court. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 372 (1996). The Court must conduct an independent analysis of the disputed claim terms. It is insufficient for the Court to simply choose between the constructions proposed by the adversarial parties. *Exxon Chem. Patents v. Lubrizol Corp.*, 64 F.3d 1553, 1555 (Fed. Cir. 1995). To determine the meaning of a patent claim, the Court considers three sources: the claims, the specification, and the prosecution history. *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (*en banc*), *aff'd*, *Markman*, 517 U.S. 370.

The Court looks first to the words of the claims. *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). "Although words in a claim are generally given their ordinary and customary meaning, a patentee may choose to be his own lexicographer and use terms in a manner other than their ordinary meaning, as long as the special definition of the term is clearly stated in the patent specification or file history." *Id.* (citation omitted). "A technical term used in a patent document is interpreted as having the meaning that it would be given by persons experienced in the field of the invention, unless it is apparent from the patent and the prosecution history that the inventor used the term with a different meaning." *Hoechst Celanese Corp. v. BP Chems. Ltd.*, 78 F.3d 1575, 1578 (Fed. Cir. 1996). The doctrine of claim differentiation creates the presumption that limitations stated in dependent claims are not to be read into the independent claim from which they depend because different language used in separate claims is presumed to indicate that the claims have different meanings and scope. *Tandon Corp. v. U.S. International Trade Com.*, 831 F.2d 1017,

United States District Court
For the Northern District of California

1023 (Fed. Cir. 1987).

Second, it is always necessary to review the specification to determine whether the inventor has used any terms in a manner inconsistent with their ordinary meaning. *Vitronics*, 90 F.3d at 1582. The specification can act as a dictionary when it expressly or impliedly defines terms used in the claims. *Id.* Because the specification must contain a description of the invention that is clear and complete enough to enable those of ordinary skill in the art to make and use it, the specification is the single best guide to the meaning of a disputed term. *Id.* The written description part of the specification itself does not delimit the right to exclude, however; that is the function and purpose of claims. *Markman*, 52 F.3d at 980.

Third, the court may consider the prosecution history. *Vitronics*, 90 F.3d at 1582. "Although the prosecution history can and should be used to understand the language used in the claims, it too cannot enlarge, diminish, or vary the limitations in the claims." *Markman*, 52 F.3d at 980 (internal quotation marks deleted) (citations omitted). However, a concession made or position taken to establish patentability in view of prior art on which the examiner has relied, is a substantive position on the technology for which a patent is sought, and will generally generate an estoppel. In contrast, when claim changes or arguments are made in order to more particularly point out the applicant's invention, the purpose is to impart precision, not to overcome prior art. Such prosecution is not presumed to raise an estoppel, but is reviewed on its facts, with the guidance of precedent. *Pall Corp. v. Micron Separations, Inc.*, 66 F.3d 1211, 1220 (Fed. Cir. 1995) (citations omitted).

Ordinarily, the Court should not rely on expert testimony to assist in claim construction, because the public is entitled to rely on the public record of the patentee's claim (as contained in the patent claim, the specification, and the prosecution history) to ascertain the scope of the claimed invention. *Vitronics*, 90 F.3d at 1583. "[W]here the public record unambiguously describes the scope of the patented invention, reliance on any extrinsic evidence is improper." *Id.* Extrinsic evidence should be used only if needed to assist in determining the meaning or scope of technical terms in the claims, and may not be used to vary or contradict the terms of the claims. *Id.* (quoting *Pall Corp.*, 66 F.3d at 1216); *Markman*, 52 F.3d at 981.

The Court is free to consult technical treatises and dictionaries at any time, however, in order

United States District Court
For the Northern District of California

to better understand the underlying technology and may also rely on dictionary definitions when construing claim terms, so long as the dictionary definition does not contradict any definition found in or ascertained by a reading of the patent documents. *Vitronics*, 90 F.3d at 1584 n.6. The Court also has the discretion to admit and rely upon prior art proffered by one of the parties, whether or not cited in the specification or the file history, but only when the meaning of the disputed terms cannot be ascertained from a careful reading of the public record. *Id.* at 1584. Referring to prior art may make it unnecessary to rely on expert testimony, because prior art may be indicative of what all those skilled in the art generally believe a certain term means. *Id.* Unlike expert testimony, these sources are accessible to the public prior to litigation to aid in determining the scope of an invention. *Id.*

Disputed claim terms are construed consistently across all claims within a patent. *Southwall Techs., Inc. V. Cardinal IG Co.*, 54 F.3d 1570, 1579 (Fed. Cir. 1995). Where patents-in-suit share the same disclosures, common terms are construed consistently across all claims in both patents. *Mycogen Plant Sci., Inc. v. Monsanto Co.*, 252 F.3d 1306, 1311 (Fed. Cir. 2001) (*overruled on other grounds*).

"The subjective intent of the inventor when he used a particular term is of little or no probative weight in determining the scope of a claim (except as documented in the prosecution history)." *Markman*, 50 F.3d at 985 (citation omitted). "Rather the focus is on the objective test of what one of ordinary skill in the art at the time of the invention would have understood the term to mean." *Id.* at 986.

DISPUTED CLAIM TERMS

The following is a list of ten terms identified by the parties in the October 21, 2004 Joint Submission of Terms, Phrases, and Clauses for Claims Construction:

1) **A computer-aided design process for designing**

2) **architecture independent actions and conditions**

3) **a set of definitions of architecture independent actions and conditions**

4) **describing . . . a series of architecture independent actions and conditions**

5) **expert system knowledge base**

6) **a set of cell selection rules**

United States District Court
For the Northern District of California

7) selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell

8) said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed

9) specifying for each described action and condition of the series one of said stored definitions

10) a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit

ANALYSIS

A. *A computer-aided design process for designing*

Ricoh contends that the term means "during manufacture of a desired application specific integrated circuit (ASIC) chip . . . a process of designing the desired ASIC using a computer." Aeroflex Inc. and Synopsys, Inc. ("Aeroflex") state that the term means "a process that uses a computer for designing, as distinguished from a computer-aided manufacturing process, which uses a computer to direct and control the manufacturing process." In essence, the parties' fundamental disagreement revolves around whether the computer-aided design process described in claim 13 also encompasses the ASIC manufacturing process.

Ricoh bases it proposed construction on the text of the patent specification. Specifically, Ricoh directs the Court to language in the specification that states that "the present invention, for the first time, opens the possibility for *the design and production* of ASICs by designers, engineers and technicians who may not possess the specialized expert knowledge of a highly skilled VLSI design engineer." '432 patent, col. 2:15-20 (emphasis added). Ricoh also emphasizes that the present invention produces a "physical chip layout level description [that] provides the mask data needed for fabricating the chip." '432 patent, col. 1:42-44; *see also* '432 patent, col. 3:68 - 4:4 ("FIG. 1c illustrates a physical layout level representation of an integrated circuit design, which provides the detailed mask data necessary to actually manufacture the devices and conductors which together comprise integrated circuit.").

Aeroflex argues that Ricoh's proposed construction is contrary to the '432 patent's claims

and specifications.[1] Specifically, Aeroflex focuses on the claim language that provides that the invention is a "computer-aided design process for designing . . . ." '432 patent, col. 16:34. Aeroflex also directs the Court to specification language that states the invention "relates to the design of integrated circuits, and more particularly relates to a computer-aided method . . . for designing integrated circuits."[2] '432 patent, col. 1:9-12.

Ricoh's proposed definition is problematic because it clearly attempts to blur the line between the process of designing integrated circuits and the process of manufacturing integrated circuits. Nothing in the claim language supports Ricoh's attempt to broaden the claims to include a manufacturing process for a desired ASIC. Rather, the claim language describes a "computer-aided design process for designing an [ASIC] . . . ." '432 patent, col. 16:34-35. Likewise, the specification consistently describes a design, rather than a manufacturing, process. In fact, the term "manufacture" does not appear in the claim or specification language.[3] While the "netlist" may be required to "produce the particular [ASIC]," *see* '432 patent, col. 2:44-49, that does not compel the conclusion that the '432 patent's design process is inherently a part of the manufacturing process of the actual ASIC chips. Given the Court's "focus . . . on the objective test of what one of ordinary skill in the art at the time of the invention would have understood the term to mean," *Markman*, 50 F.3d at 985, the Court finds that the "computer-aided design process" described in claim 13 does not include a

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[1]Aeroflex also argues that Ricoh's proposed construction is contrary to statements made in the '432 patent's file history. Specifically, the April 1989 Amendment provides: "The present invention is a computer-aided design . . . method whereby the use can design application specific integrated circuits . . . ." (April 1989 Amendment at 8).

[2]Aeroflex also argues that its proposed construction is more consistent with the '432 patent's title: "Knowledge Based Method and Apparatus For *Designing* Integrated Circuits Using Functional Specifications" (emphasis added).

[3]In its reply, Ricoh focuses solely on the specification language that states "the present invention, for the first time, opens the possibility for the design *and production* of ASICs by designers, engineers and technicians who may not possess the specialized expert knowledge of a highly skilled VLSI design engineer." '432 patent, col. 2:15-20 (emphasis added). However, this language, standing alone, does little to persuade the Court that the present invention was intended to encompass the ASIC manufacturing process. Rather, a fair reading of this language is that the present invention simply opened up the "possibility" that non-experts could produce or manufacture ASICs at some point in the future, but not that the present invention currently encompassed such a process.

United States District Court
For the Northern District of California

manufacturing process for ASICs.[4]

Given these considerations, the clearest reading of "A computer-aided design process for designing" is *a process that uses a computer to direct and control the design of an ASIC chip.*

B. *architecture independent actions and conditions*

Ricoh contends that the term means "functional or behavioral aspects of a portion of a circuit (or circuit segment) that does not imply any set architecture, structure or implementing technology." Aeroflex states that the term means "the logical steps and decisions that are represented as rectangles and diamonds in the flowchart; where register-transfer level (RTL, as defined in Darringer et al.) descriptions are excluded." Thus, the parties disagreement focuses on whether claim 13 limits input specifications for the proposed ASIC to data in a flowchart format.

Ricoh admits that Fig. 1a illustrates an embodiment that utilizes a flowchart representation. However, Ricoh argues that Aeroflex's definition impermissibly attempts to limit the scope of the claimed invention to the preferred embodiment of the '432 patent. Ricoh contends that a broader interpretation of "architecture independent actions and conditions" is supported by the patent specification:

> The architecture independent functional specifications can be defined in a suitable manner, *such as in list form* or preferably in a flowchart form. The flowchart is a highly effective means of describing a sequence of logical operations, and is well understood by software and hardware designers of varying levels of expertise and training. From the flowchart (*or other functional specifications*), the system and method of the present invention translates the architecture independent functional specifications into an architecture specific structural level definition of an integrated circuit, which can be used directly to produce the ASIC.

'432 patent, col. 2:21-34 (emphasis added).[5] Ricoh also relies on specification language stating that "the present invention . . . enables a user to define the functional requirements for a desired target integrated circuit, using an easily understood architecture independent functional level representation . . . ." '432 patent, col. 2:6-11. Ricoh also notes that patent claim 11, not patent claim 13,

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[4]This conclusion is also bolstered by the language in claim 14. Claim 14 describes "[a] process as defined in claim 13, including generating from the netlist the mask data required to produce an integrated circuit having the desired function." '432 patent, col. 16:66-68. This language clarifies that the generation of the netlist (the final step in claim 13) and the production of the integrated circuit are two distinct processes.

[5]Ricoh argues that a "list form" input specification is a preferred embodiment of the '432 patent. However, this argument does not find any support in the patent specification.

United States District Court
For the Northern District of California

specifically references a flowchart format and recites "having boxes representing architecture independent actions" and "diamonds representing architecture independent conditions." '432 patent, col. 16:10-12. Ricoh argues that this demonstrates that if the patentee intended the use of "architecture independent" in claim 13 to be restricted to a flowchart format, the patentee would have used the same or similar limiting language as used in claim 11.

Aeroflex responds that the '432 patent's file history conclusively demonstrates that claim 13 requires a sequence of logical steps and decisions in a flowchart format.[6] *See* April 1989 Amendment at 11; October 1989 Examiner Interview Summary; November 1989 Amendment at 7. Aeroflex contends that the Examiner Interview Summary explicitly states that the examiner and the applicant reached an agreement on application term 20 (patent claim 13). Specifically, the Examiner Interview Summary form shows that the examiner checked the box providing: "Agreement was reached with respect to some or all of the claims in question." (October 1989 Interview Summary). The summary form identifies application claim 20 (patent claim 13) as one of the claims discussed, and states that the following agreement was reached: "It is agreed that the features 'flowchart editor' and 'expert system for translating the flowchart into a netlist defining the necessary hardware cells of the integrated circuit' are patentable [sic] distinct from the reference list above." Aeroflex argues that this language demonstrates that an agreement was reached and that the features "flowchart editor" and "expert system for translating the flowchart into a netlist" were the examiner's only basis for allowing all of the claims including patent claim 13. Furthermore, Aeroflex contends that the file history demonstrates that all register-transfer level descriptions were explicitly excluded from the claimed invention.

Ricoh responds that the October Interview summary, at best, is ambiguous and inconclusive. Ricoh states that while the Interview summary clearly identified the claims discussed in the interview, it specifically left undefined which claims were subject to any agreement reached because the form indicated that an agreement was reached as "to some or all of the claims." Thus, Ricoh

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[6]Aeroflex's reliance on the specification language to support its argument is not well taken. Aeroflex cites almost exclusively to language from the preferred embodiment. *See* '432 patent, col. 3:50-59; 4:5-22, 4:35-38, 7:12-23. However, in construing disputed claim terms, a limitation cannot be imported from the preferred embodiment into the claims themselves. *Markman*, 52 F.3d at 980.

United States District Court
For the Northern District of California

concludes that the only thing evidently agreed upon was that the features of a "flowchart editor" and an "expert system" were distinct over prior art, and any claims containing those features would be understood by both parties to be patentable over the cited prior art. Ricoh contends that this understanding is supported in the November 1989 Amendment, in which the patentee stated as follows:

> During the interview, the Examiner carefully reconsidered the prior art and applicants' claims, and upon reconsideration agreed that certain features as defined in applicants' claims, such as the "flowchart editor" and the "expert system for translating the flowchart into a netlist defining the necessary hardware cells of the integrated circuit" patentably distinguish applicants' invention from the prior art of record, including Darringer et al. 4,703,435. Thus, it was agreed that Claim 18 [patent claim 11] in its present form, for example, patently defines applicants' invention over the prior art of record.

November 1989 Amendment at 7. Ricoh argues that the patentee could have made a similar statement with respect to application claim 20 (patent claim 13). Furthermore, Ricoh argues that Aeroflex's attempt to exclude register-level transfer descriptions from the claimed invention improperly distorts the file history.

Initially, the Court finds that the specification language supports Ricoh's arguments. While the flowchart format input specification is the single embodiment of the '432 patent, the specification explicitly contemplated alternative input descriptions. *See* '432 patent, col. 2:21-24; 2:27-28. "[I]t is improper to read limitations from a preferred embodiment described in the specification – even if it is the only embodiment – into the claims absent a clear indication in the intrinsic record that the patentee intended the claims to be so limited." *Liebel-Flarshiem Co. v. Medrad, Inc.*, 358 F.3d 898, 913 (Fed. Cir. 2004). Given the explicit patent language, the Court finds that the specification language does not support the conclusion that the input specification of the claimed invention is limited to a flowchart format.

Furthermore, the Court is not persuaded that the prosecution history unmistakably demonstrates that the input specification of the claimed invention is limited to the designer's use of a flowchart format. As noted by Ricoh, the October Interview Summary specifically left undefined which claims were subject to any agreement between the patentee and the examiner. Thus, contrary to Aeroflex's

United States District Court
For the Northern District of California

argument, this case is distinguishable from cases such as *Spring Window Fashions LP v. Novo Industries, L.P.*, 323 F.3d 989 (Fed Cir. 2003), in which the court held that a reasonable competitor could rely on unequivocal statements of disclaimer made during the prosecution history. Here, the statements made during the prosecution history upon which Aeroflex attempts to rely, are at best, ambiguous.

In addition, while the patentee and the examiner evidently agreed that the features of a "flowchart editor" and an "expert system" were distinct over prior art, there is no indication that those terms necessarily applied to application term 20 (patent claim 13). Moreover, the fact that those terms were not included in the final version of patent claim 13 suggests just the opposite. "To be given effect, a disclaimer must be 'clear and unmistakable.'" *Sunrace Roots Enter. Co. v. SRAM Corp.*, 336 F.3d 1298, 1306 (Fed. Cir. 2003) (quoting *Omega Eng'g, Inc. v. Raytek Corp.*, 334 F.3d 1314, 1325 (Fed. Cir. 2003)). While Aeroflex's interpretation of the October Interview summary may be reasonable, the law requires much more. Accordingly, "because the statements in the prosecution history are subject to multiple reasonable interpretations, they do not constitute a clear and unmistakable departure from the ordinary meaning of the [claim term at issue]." *Golight, Inc. v. Wal-Mart Stores, Inc.*, 355 F.3d 1327, 1332 (Fed. Cir. 2004).

Aeroflex's argument pertaining to the file history of register-transfer level descriptions is more persuasive. The file history demonstrates that the patentee amended the patent claims to include the phrase "architecture independent," and distinguished the claimed invention from prior art partially on that basis. *See* November 1989 Amendment at 7. The patentee stated that the "specifications used by Darringer et al. are not truly at an architecture independent level, but rather are at a lower level which is indeed hardware architecture dependent and defines the system at a 'register-transfer' level description." *Id.* Similarly, in the April 1989 Amendment, the patentee stated that "a very clear distinction between Darringer and the present invention is that the input to the Darringer system is in the form of a register transfer level flowchart control language . . . . [and] input to the present invention is in the form of an architecture independent functional specification." *Id.* Based on this language, Aeroflex argues that Ricoh disclaimed the "register-transfer" level descriptions described in the Darringer prior art from the scope of its claimed invention. Ricoh

United States District Court
For the Northern District of California

responds that the patentee's use of the term "register-transfer level" was merely a shorthand reference used to denote the "structural" RTL-type, as opposed to "functional" RTL-type, of input systems prevalent at the time.

In order to make this determination, the Court must examine the Darringer 4,704,435 Patent ("the '435 patent") and how closely it reads upon the present invention. The '435 patent specifically defines a register-transfer level description and the subsequent translation or transformation steps described in that patent do not alter this explicit definition.[7] '435 patent, col. 5:27-38. The Court finds no relevant distinction between the RTL described in the '435 patent and the RTL specifically disclaimed by Ricoh in the April and November 1989 Amendments. Furthermore, an examination of the '432 patent's public record fails to provide any support for Ricoh's distinction between "structural" and "functional" RTL-type input systems. Given these findings, Ricoh's attempt to limit the patentee's disclaimer to only "structural" level RTL-type input systems is unpersuasive. *See Kumar v. Ovonic Battery Co.*, Inc., 351 F.3d 1364, 1368 (Fed. Cir. 2003) (adopting definition of term in cited prior art which is intrinsic evidence). Accordingly, the prosecution history indicates that the patentee expressly disclaimed all register-transfer level descriptions.

Given these considerations, the Court defines "architecture independent actions and conditions" as *functional or behavioral aspects of a portion of a circuit (or circuit segment) that does not imply a set architecture, structure, or implementing technology, but excludes the use of register-transfer level descriptions as taught in Darringer.*

C. ***a set of definitions of architecture independent actions and conditions***

Ricoh contends that the term means "a library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC." In contrast, Aeroflex proposes that the term means "a set of named descriptions defining the functionality and arguments for the available logical steps and decisions that may be specified in the flowchart where

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[7] "[T]he process of this invention begins at step 100 with a register-transfer level description e.g. of the type shown in Fig. 4. The description consists of two parts: a specification of the inputs, outputs and latches of the chip to be synthesized; and a flowchart-like specification of control, describing for a single clock cycle of the machine how the chip outputs and latches are set according to the values of the chip inputs and previous values of the latches. At step 102 in FIG 2., the register-transfer level description undergoes a simple translation to an initial implementation of AND/OR logic. '435 patent, col. 5:27-38.

United States District Court
For the Northern District of California

register-transfer level (RTL, as defined in Darringer et al.) descriptions are excluded."

It appears that the parties real dispute centers, once again, around the term "architecture independent actions and conditions." This phrase should be construed as explained *supra*. It does not appear that the Court needs to construe "a set of definitions," as this term should be given its ordinary and customary meaning. To the extent that "a set of definitions" needs to be construed by the Court, Aeroflex's Responsive Brief is unhelpful because it never addresses Ricoh's proposed construction. It appears that Aeroflex's use of the terms "named descriptions" and "arguments" intends to encompass the "macros" shown in Table 1 of the '432 patent. *See* '432 patent, col. 7:29-49. Given Aeroflex's lack of analysis of this term, the Court cannot accept Aeroflex's definition as it has not presented a basis for narrowing the claim term. Ricoh's use of the term "library" is supported by the patent's intrinsic evidence. *See* '432 patent, col. 2:20-22. Thus, the Court construes "a set of definitions of architecture independent actions and conditions" as *a library of definitions of the different architecture independent actions and conditions that can be selected for use in the desired ASIC.*

D. *describing . . . a series of architecture independent actions and conditions*

Ricoh contends that the term means "a user describing an input specification containing the desired functions to be performed by the desired ASIC." Aeroflex states that the term means "the designer represents a sequence of logical steps (rectangles) and decisions (diamonds), and the transitions (lines with arrows) between them in a flowchart format that excludes any register-transfer level (RTL, as defined in Darringer et al.) descriptions.

Once again, it appears that the parties real dispute centers around the term "architecture independent actions and conditions." This phrase should be construed as explained *supra* and is not limited to the use of a "flowchart format." To the extent that the terms "describing" and "series" need to be defined, they should be given their ordinary and customary meaning. "Describe" is defined as "to represent or give an account in words." Merriam-Webster's Ninth New Collegiate Dictionary (1987). The parties have not provided the Court with the ordinary meaning of the term "series."

Aeroflex argues that Ricoh's proposed construction is contrary to the claim language because

United States District Court
For the Northern District of California

it merely requires an input specification "containing the desired functions," and thus eliminates the requirement that the designer must describe "a series." Aeroflex contends that such a definition contradicts the actual words in the claim (i.e., "describing . . . a series) and is also contrary to the requirement in the patent's specification that the designer must "describ[e] a sequence of logical operations." '432 patent, col. 2:24-25. Ricoh does not address this argument. Accordingly, the Court defines "describing . . . a series of architecture independent actions and conditions" as *describing an input specification containing a series of desired functions to be performed by the desired ASIC.*

E. *expert system knowledge base*

Ricoh contends that the term means "a database used to store expert knowledge of highly skilled VLSI designers." Aeroflex defines "expert system" and "knowledge base" separately. Aeroflex states that "expert system" should be defined as "software that solves problems through selective application of the rules in the knowledge base by an inference engine, as distinguished from conventional software, which uses a predefined step-by-step procedure (algorithm) to solve problems." Aeroflex asserts that a knowledge base is a "portion of the expert system software having a set of rules, each rule having an antecedent portion (e.g. IF) and a consequent portion (e.g., THEN), and embodying the knowledge of expert designers for application specific integrated circuits."

Ricoh's proposed construction relies heavily on the '432 patent's specification. Specifically, the specification states that "[t]he knowledge base 35 contains ASIC design expert knowledge required for data path synthesis and cell selection." '432 patent, col. 5:6-8. "Using a rule based expert system with a knowledge base 35 extracted from expert ASIC designers, the KBSC system selects from the cell library 34 the optimum cell for carrying out the desired function." '432 patent, col. 5:25-29. Based on these passages, Ricoh argues that an "expert system knowledge base" is a collection of data that represents knowledge obtained from experts in ASIC design.

Aeroflex dismisses Ricoh's proposed construction as overly simplistic. Aeroflex argues that a person of ordinary skill in the art in 1988 would have known that two distinct approaches existed for selecting hardware cells: 1) rule-based expert system software; and 2) conventional algorithmic

United States District Court
For the Northern District of California

software. Aeroflex further contends that a person of ordinary skill in the art would have understood that rule-based expert system software must contain an inference engine, a knowledge base, and a working memory, which enable the inference engine to selectively apply the rules stored in the knowledge base to what is stored in the working memory (as distinguished from conventional algorithmic software, which uses a predefined step-by-step procedure). To support its argument, Aeroflex cites to a technical dictionary entitled "Artificial Intelligence Terminology" that states: "An expert system will generally consist of a rule base, an inference engine and a user interface (which will generally provide an explanation facility)." Aeroflex also cites the Court to the Dunn Patent 4,656,603 ("the '603 patent"). The '603 patent speaks in general terms regarding the distinction between the two types of software and states that since rule-based expert systems "often must make conclusions based on incomplete or uncertain information, they differ substantially from conventional computer programs which solve problems in accordance with pre-defined algorithms and complete data sets." '603 patent, col. 1:44-49.

Aeroflex also argues that the distinction between the rule-based expert system approach and the conventional algorithmic approach is evident from the prior art that the patentee distinguished in the patent's file history. In the November 1989 Amendment, the patentee added the following language to application claim 5 (patent claim 1): "said cell selection means comprising an expert system including a knowledge base containing rules for selecting hardware cells from said cell library and inference engine means for selecting appropriate hardware cells from said cell library in accordance with the rules of said knowledge base." November 1989 Amendment at 2. The patentee stated that application claim 5 (patent claim 1) was amended to "clearly distinguish it over the cited prior art by more clearly defining the expert system aspects of applicant's invention including the provision of a knowledge base containing rules for selecting hardware cells, inference engine means for selecting appropriate hardware cells, and netlist generator means for generating a netlist defining the hardware . . . ." November 1989 Amendment at 8. Although this amendment applied only to application claim 5 (patent claim 1), the patentee also amended application claim 20 (patent claim 13) to include "applying . . . a set of cell selection rules stored in said expert system knowledge base . . . ." The patentee explained that this language was added to "emphasize the expert system aspects

United States District Court
For the Northern District of California

of applicants' method." November 1989 Amendment at 9. Thus, Aeroflex is essentially arguing that the description of an expert system in patent claim 1 (including an inference engine) should also be read to encompass the expert system described in patent claim 13.

Ricoh responds that the patentee's statement in the November 1989 Amendment only further proves its point. Ricoh argues that this statement does not establish that an "expert system" had become an element of claim 13, but merely confirmed the patentee intent to claim certain aspects (i.e., the claimed "expert system knowledge base") of an expert system - not an expert system itself.[8] Moreover, Ricoh argues that even if the Court finds that the patentee intended to encompass both an "expert system" and a "knowledge base," there is nothing in the claim language, specification, or prosecution history that requires that an expert system contain an inference engine and a working memory.

Initially, the Court finds no support for Ricoh's argument that "expert system" is simply an adjective modifying the noun "knowledge base." The patentee explicitly stated that claim 13 was "amended to emphasize the expert system aspects of applicant's method." November 1989 Amendment at 9. Therefore, the Court finds that "expert system" was an element of claim 13.

Next, the Court finds that Aeroflex's assertion that a person of ordinary skill in the art would have understood that rule-based expert system software must contain an inference engine, a knowledge base, and a working memory is simply not supported by the intrinsic evidence. As noted by Ricoh, claims one through nine of the '432 patent specifically claim an inference engine, while claim 13 does not make such a claim. Aeroflex's attempt to have the Court read the description of an expert system from patent claim 1 onto the expert system described in patent claim 13 is unpersuasive. Additionally, the technical dictionary definition provided by Aeroflex states that an inference engine is "generally" an element of an expert system. Given the qualified language of the definition, in combination with the fact that claim 13 makes no mention of an "inference engine," the Court finds the technical dictionary definition unhelpful in this context. Finally, Aeroflex's reference to the '603 patent is ultimately unhelpful, as the '603 patent describes an intentional expert

[8]In other words, Ricoh is arguing that the term "expert system" is grammatically read as an adjective or other modifier for the noun "knowledge base."

United States District Court
For the Northern District of California

system, as opposed to a knowledge-based expert system, and makes no mention of an inference engine. '603 patent, col. 5:53-56. Given these considerations, the Court defines "expert system" and "knowledge base" separately. "Expert system" should be defined as *software that solves problems through selective application of rules in the knowledge base.* "Knowledge base" should be defined as a *portion of an expert system software having a set of rules and embodying expert knowledge of highly skilled VLSI designers.*

F. ***a set of cell selection rules***

Ricoh contends that the disputed term is defined as "a plurality of rules for selecting among the hardware cells from the hardware cell library, wherein the rules comprise the expert knowledge of highly skilled designers formulated as prescribed procedures." Aeroflex contends that the term is properly defined as "a set of rules embodying the knowledge of expert designers for application specific integrated circuits, each rule having an antecedent portion (e.g. IF) and a consequent portion (e.g., THEN), which enables the expert system to map the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description."

Aeroflex states that its proposed construction is consistent with contemporaneous technical dictionaries, treatises, and the prior art. *See* Ex. 15 at 74-75, Ex. 17 at 10-11, Ex. 14 at 10, 53, Ex. 18 at 8, Ex. 20 at 14-15, Ex. 21 at 269. "The two parts of a rule are a premise and a conclusion, a situation and an action, or an antecedent and a consequent. These statements are written in an IF-THEN format." Ex. 15 at 74, Louis E. Frenzel Jr., *Understanding Expert Systems.* The technical dictionary provided by Aeroflex defines "rule" as follows: "(If-Then Rule). A conditional statement of two parts." Ex. 21, Paul Harmon, *Expert Systems: Tools & Applications.* Aeroflex also argues that the patent's specification requires that the "rules" not only embody expert knowledge, but that the expert knowledge also be used for mapping the specified definitions in the flowchart to the hardware cell descriptions. Aeroflex Responsive Brief at 48; *see* '432 patent, col. 8:21-23; 8:34-37.

Ricoh contends that the general usage dictionary definition of "rule" should apply. Also, while Ricoh admits that the preferred embodiment of the '432 patent disclosed that "rules" could be in the format of "an antecedent portion (IF) and a consequent portion (THEN)," it also asserts that

United States District Court
For the Northern District of California

nothing in the public record justifies restriction of the claimed "rules" to the exemplary format disclosed as the preferred embodiment. Richo additionally contends that the '432 patent states specific rules in the specification that are not stated in the if/then format. *See* '432 patent, col. 12:31-35. Moreover, Ricoh also disagrees with Aeroflex's inclusion of the following requirement: "embodying the knowledge of expert designers for application specific circuits." Ricoh argues that to the extent Aeroflex is attempting to create a distinction between the knowledge of designers for ASICs and the knowledge of designers skilled in VLSI design, the claim should be construed broadly to include either skill. *See, e.g.*, '432 patent, col. 2:58-61 ("The KBSC utilizes a knowledge based expert system, with a knowledge base extracted from expert ASIC designers with a high level of expertise in VLSI design . . ."); col. 4:8-11 ("In the KBSC system of the present invention, however, integrated circuits can be designed at a functional level because the expertise in VLSI design is provided and applied by the invention.")

Based on Aeroflex's citation to the technical dictionary, it appears that "rule" as used in the '432 patent would have had a particular meaning to one of ordinary skill in the art. Therefore, to the extent Ricoh's definition relies on a general dictionary definition, it must be rejected. *See Vanderlande Industries Nederland BV v. I.T.C.*, 366 F.3d 1311, 1321 (Fed. Cir. 2004). The technical dictionary definition offered by Aeroflex demonstrates that the ordinary meaning of "rules" when used to refer to rules that are contained in the knowledge base of a rule-based expert system must include an "IF-THEN" component. The Court is not persuaded that column 12, lines 31 to 35 of the '432 patent state "rules" as that term is understood in the patent. Rather, lines 31 to 35 appear to be discussing other actions that a user could take if additional rules were present.

However, the Court finds little support for Aeroflex's argument that claim 13 requires that the rules stored in the knowledge base of the rule-based expert system embody the expert knowledge for mapping the specified definitions in the flowchart to the hardware cell descriptions. Certainly, the plain language of claim 13 does not dictate that the "rules" encompass the "mapping" function. Moreover, while the patent's specification does suggest that the rules might play such a role in the preferred embodiment, *see* '432 patent, col. 8:34-37, such a conclusion is not compelled from the specification language. In any event, the Court should not "limit[] the claimed invention to preferred

United States District Court
For the Northern District of California

embodiments or specific examples in the specification." *Ekchian v. Home Depot, Inc.*, 104 F.3d 1299, 1303 (Fed. Cir. 1997).

Furthermore, Ricoh correctly states that the definition should not make a distinction between the knowledge of designers for ASICs and the knowledge of designers skilled in VLSI design. The specification clearly contemplated that both sets of knowledge would be included in the knowledge base. *See* '432 patent, col. 2:58-61; col. 4:8-11. Furthermore, Aeroflex's attempt to include the following language in the definition - "for each logical step and decision represented in the flowchart" - should be rejected for the reasons discussed *supra*. Accordingly, the Court construes "a set of cell selection rules" as *a set of rules embodying the expert knowledge of highly skilled VLSI designers, each rule having an antecedent portion (e.g., IF) and a consequent portion (e.g. THEN).*

G. ***selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell***

Ricoh contends that the term means "selecting from the plurality of hardware cells in the hardware cell library a hardware cell for performing the desired function of the desired ASIC." Aeroflex contends that the term means "mapping the specified stored definitions for each logical step and decision represented in the flowchart to a corresponding stored hardware cell description."

Ricoh's argues that this term simply refers to the process of selecting hardware cells from those stored in the hardware cell library that can be used to implement the desired functions of the ASIC to be produced. In support of its argument, Ricoh cites the specification language stating that "[t]he Cell Selector 32 is a knowledge based system for selecting a set of optimum cells from the cell library to implement a VLSI system." '432 patent, col. 8:21-23.

Aeroflex argues that its proposed construction is supported by the language in claim 13, which according to Aeroflex, "dictates that mapping the specified definitions to the stored hardware cell descriptions must be performed by a rule-based expert system and not conventional software." Aeroflex Responsive Brief at 41:3-6. Aeroflex relies upon the following specification language to support its argument: "To design a VLSI system from a flowchart description of a user application, it is necessary to match the functions in a flowchart with cells from a cell library. This mapping needs the use of artificial techniques because the cell selection process is complicated and is done on the

United States District Court
For the Northern District of California

basis of a number of design parameters and constraints." '432 patent, col. 8:31-31-37.

Although it is a close question, Aeroflex's argument is ultimately more compelling. As discussed above, the patent file history demonstrates that the patentee distinguished the present invention based on the rule-based expert system's ability "to accomplish a task of selection of cells from the cell library." April 1989 Amendment at 10. This amendment strongly suggests that the mapping of the specified definitions to the stored hardware cells must be performed by a rule-based system. *See* Aeroflex Responsive Brief at 42. Ricoh's proposed language does not include a reference to a "rule-based system." Aeroflex's use of the word "mapping" is supported by the specification language '432 patent, col. 8:34; col. 9:53. Furthermore, at the claims construction hearing, Ricoh's counsel stated that he had no objection to the use of the term "mapping" in this context. However, Aeroflex's inclusion of the phrase "for each logical step and decision represented in the flowchart" is improper because it attempts to limit the claim to the preferred embodiment of the flowchart input specification, as discussed *supra*. Therefore, the Court construes "selecting from said stored data for each of the specified definitions a corresponding integrated circuit hardware cell" as *mapping the specified stored function to a corresponding stored hardware cell.*

H. said step of selecting a hardware cell comprising applying to the specified definition of the action or condition to be performed

Ricoh argues that the term is defined as "selecting from the plurality of hardware cells in the hardware cell library a hardware cell . . . through application of the rules; and generating a netlist that identifies the hardware cells needed to perform the function of the desired ASIC." Aeroflex contends that the term should be defined as "the mapping of the specified definitions to the stored hardware cell descriptions must be performed by applying to the specified definitions in the flowchart a set of cell selection rules stored in an expert system knowledge base."

The parties proposed constructions are not substantially different. As discussed above, Aeroflex's attempt to restrict the term to "definitions in the flowchart" is incorrect. However, Aeroflex's proposed use of the term "expert system knowledge base" also seems incorrect because it is unnecessary here; the term does not require a definition that specifies the location where the cell selection rules are found. Similarly, Ricoh's inclusion of "generating a netlist that identifies the

United States District Court
For the Northern District of California

hardware cells needed to perform the function of the desired ASIC" seems unnecessary here; such a definition would function to incorporate a separate step of the claim not covered by the current term. Accordingly, the Court defines the term as *the mapping of the specified definitions to the stored hardware cell descriptions by applying to the specified definitions a set of cell selection rules.*

I. *specifying for each described action and condition of the series one of said stored definitions*

Ricoh proposes that this term be construed as "specifying for each desired function to be performed by the desired ASIC one of the definitions of the architecture independent actions and conditions stored in the library of definitions that is associated with the desired function." Aeroflex contends that the proper construction of the term is "the designer assigns one definition from a set of stored definitions to each of the logical steps and decisions represented in the flowchart." The parties dispute centers around whether the "specifying" step must be performed manually by a user, or whether the assignment of macros can be done automatically.

Ricoh admits that the patent discloses a "manual mapping" embodiment. '432 patent, col. 7:24-25 ("Edit actions allows the designer to assign actions to each box."). However, Ricoh argues that the construction of the claim should not be limited merely because it is the only embodiment disclosed. *See Liebel-Flarshiem Co.*, 358 F.3d at 913. Furthermore, Ricoh contends that the patent describes macros being "mapped" automatically through the application of rules. *See* '432 patent, col. 9:14-18. Ricoh argues that if col. 9:14-18 is read in context, the passage shows that the quoted rules are to be applied "during this stage," which refers to the "first step of cell list generation." Accordingly, Ricoh contends that this passage does not apply to a statelist in which the "macros" have already been assigned to the desired actions.

Aeroflex disagrees with Ricoh's proposed construction. First, Aeroflex argues that the prepositional phrase "for each described action and condition of the series" refers only to the fact that the "specifying" step is performed for each action and condition in the described series resulting from the previous "describing" step. Thus, Aeroflex concludes that the claim language for this "specifying" step requires that "the designer assigns one stored definition for each logical step and decision described in the flowchart." Second, Aeroflex argues that other claims demonstrate that for

United States District Court
For the Northern District of California

each action and condition described, this step requires the designer to specify one stored definition (from a macro library) and that this "specifying" step and the previous "describing" step together are the steps that define the input specification for the claimed invention's method. Third, Aeroflex argues that Ricoh's proposed construction impermissibly attempts to replace the phrase "for each described action and condition" with the phrase "for each desired function to be performed by the desired ASIC." Finally, Aeroflex argues that the '432 patent does not contain an automated "mapping" embodiment.

The Court finds that Aeroflex's attempt to limit the "specifying" step to encompass only a user manually assigning a single definition to each action and condition is too narrow of a construction. The plain language of the claim simply does not support this construction, and the Court should not "limit[] the claimed invention to preferred embodiments or specific examples in the specification." *Ekchian*, 104 F.3d at 1303. Moreover, while Aeroflex is correct that claim 1 and claim 9 require the designer to "specify" one stored definition for each action and condition described, this contention alone does not suggest that the Court should juxtapose these claims onto claim 13. Claim 13 simply does not contain similar language.[9]

Additionally Ricoh's attempt to replace the phrase "for each described action and condition" with the phrase "for each desired function to be performed by the desired ASIC" is permissible. Throughout the specification, each "action and condition" is referenced as a "function." *See* '432 patent, col. 2:21-30. Therefore, the Court construes "specifying for each described action and condition of the series one of said stored definitions" as *specifying for each desired functional specification to be performed by the desired ASIC one of the definitions from the set of stored definitions.*

J. a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit

Ricoh contends that the term means "a description of the hardware components (and their interconnections) needed to manufacture the ASIC as used by subsequent processes, e.g., mask

[9]Aeroflex's proposed construction is also flawed because of its inclusion of the phrase "logical steps and decisions represented in the flowchart." *See* discussion *supra*.

United States District Court
For the Northern District of California

development, foundry, etc." Aeroflex states that the term means "producing a list of the needed hardware cells by eliminating any mapped hardware cells that are redundant or otherwise unnecessary, producing a custom controller type hardware cell for providing the needed control for those other hardware cells, and producing the necessary structural control paths and data paths for the needed hardware cells and the custom controller." '432 patent, col. 5:38-46.

Ricoh's proposed construction also relies heavily upon language in the specification. Specifically, Ricoh notes that the specification states that "[t]he list of hardware cells and their interconnection requirements may be represented in the form of a netlist. From the netlist it is possible using either known manual techniques or existing VLSI CAD layout systems to generate the detailed chip level geometrical information (e.g. mask data) required to produce the particular application specific integrated circuit in chip form." '432 patent, col. 2:42-49. The specification also states that "[t]he netlist provides all the necessary information required to produce the integrated circuit. Computer-aided design systems for cell placement and routing are commercially available which will receive netlist data as input and will lay out the respective cells in the chip, generate the necessary routing, and produce mask data which can be directly used by the chip foundry in the fabrication of integrated circuits."

Aeroflex also relies heavily upon the patent's specification to support its proposed construction. Aeroflex initially argues that the claim language "generating for the selected . . . hardware cells, a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit" requires that this step eliminate any selected hardware cells that are not needed. *See* '432 patent, col. 13:59-66. Aeroflex also contends that the patent's specification defines the "interconnection requirements" for the necessary hardware cells defined in the netlist as "data and control paths." *See* '432 patent, col. 5:30-35. Finally, Aeroflex contends that a system controller must be generated for the netlist. In support of its argument, Aeroflex cites language from the preferred embodiment that states "[t]he netlist includes a custom generated system controller, all other hardware cells required to implement the necessary operations, and interconnection information for connecting the hardware cells and the system controller." '432 patent, col. 4:39-43. Additionally, Aeroflex asserts that the requirement that a controller be generated is also supported by

United States District Court
For the Northern District of California

the patent's file history. Specifically, Aeroflex argues that the file history limits the input specification to exclude register-transfer level descriptions that would define the control for the hardware cells of the ASIC, and thus a controller must be generated to provide necessary control for the ASIC.

The Court agrees with Ricoh that Aeroflex's arguments regarding "eliminating any mapped hardware cells that are redundant or otherwise unnecessary" and "producing a custom controller type hardware cell for providing the needed control for those other hardware cells" bear no relationship to a plain reading of claim 13. Additionally, contrary to Aeroflex's assertion, a review of the patent file history does not reveal that a controller must be generated in claim 13. Furthermore, while claim 10 expressly includes the generation of a controller, claim 13 includes no such language. *See* '432 patent, col. 16:1-4 ("The system as defined in claim 9 additionally including control generator means for generating a controller and control paths for the hardware cells selected by said cell section means.").

The Court also finds that claim 13 does not restrict the interconnection requirements of the hardware cells to "data and control paths." To be certain, "data and control paths" are the types of interconnections disclosed in the patent's preferred embodiment. But, the Court should not "limit[] the claimed invention to preferred embodiments or specific examples in the specification." *Ekchian*, 104 F.3d at 1303. Moreover, while claim 15 expressly includes the generation of control paths, claim 13 includes no such language. *See* '432 patent, col. 17:1-3 ("A process as defined in claim 13 including the further step of generating data paths for the selected integrated circuit hardware cells."). For these reasons, the Court agrees with Ricoh's proposed construction of the term. The Court defines "a netlist defining the hardware cells which are needed to perform the desired function of the integrated circuit" *as a description of the hardware components (and their interconnections) needed to manufacture the ASIC as used by subsequent processes, e.g., mask development, foundry, etc.*

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United States District Court
For the Northern District of California

CONCLUSION

Based on the analysis above, the Court adopts the foregoing constructions of the disputed claim terms.

IT IS SO ORDERED.

Dated: April 7, 2005

MARTIN J. JENKINS
UNITED STATES DISTRICT JUDGE

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

- - - - - - - - - - - - - -x

RICOH COMPANY, LTD., :

Plaintiff, :

vs. : Case No.

AEROFLEX INCORPORATED, : C-03-4669-MJJ (EMC)

et al., :

Defendants. :

_____ :

SYNOPSYS, INC., :

Plaintiff, : Case No.

vs. : C-03-289-MJJ (EMC)

RICOH COMPANY, LTD., :

Defendant :

- - - - - - - - - - - - - -x

VIDEOTAPE DEPOSITION OF MARIOS PAPAEFTHYMIOU

Washington, DC

Friday, August 11, 2006

REPORTED BY: ERIN AVERY, RPR

BY MS. DE MORY:

Q What were the first names?

A Michael and Amanda, Rebecca. These are all the names I remember.

Q Prior to -- going back just a minute. Prior to the time that you were retained as a consultant on August 29th of 2005, had you discussed the Synopsys tools at issue in this litigation with anyone from Dickstein Shapiro?

A No.

Q So prior to August 29th of 2005, you did not discuss with Dickstein Shapiro anything about Design Compiler or HDL Compiler; is that correct?

A That is my recollection.

Q When was the first time you discussed anything about Design Compiler or HD Compiler with Dickstein Shapiro?

MS. ALLEN: Objection to the extent any -- go ahead. You asked the one question. I'll withdraw my objection.

THE WITNESS: I don't remember exact.

BY MS. DE MORY:

Q Prior to being retained as a consultant in this case, had you used Design Compiler or HDL Compiler?

A Personally, I have not used Design Compiler or HDL Compiler. My students do all the time. We talk about it all the time with my students. That's what my teaching and research to some extent is about.

Q At some point in time, did you discuss with Dickstein Shapiro your knowledge of the types of inputs that could be accepted by HDL Compiler and Design Compiler?

A Yes.

Q And what's the basis for -- what was the basis for your knowledge about the types of inputs that could be accepted by HDL Compiler and Design Compiler?

A What do you mean by basis of my knowledge?

Q Did you have knowledge about that before you were retained as a consultant?

A Yes, I was aware of the kinds of inputs that you can provide, tools like Design Compiler.

Q When you say tools like Design Compiler, what do you mean?

A Design Compiler is an EDA tool. It is an electronic design automation tool for designing chips, semiconductor chips.

Q What other tools are you aware of that are

quote/unquote, functional RTL or not.

A I was not asked to formulate an opinion about that.

Q As you sit here today, do you have an opinion about whether or not the customer designs at issue in this litigation are structural RTL?

A I was not asked to formulate an opinion about that.

Q And therefore you have no opinion about that; is that correct?

A At this point, I have not considered the question.

Q And the same is true with regard to the functional RTL question, just so that the record's clear.

As you sit here today, you've not been asked to formulate an opinion about whether or not the customer designs at issue in this litigation are functional RTL, and therefore you have no opinion on that as you sit here today?

A That is correct. At this point I have not formulated an opinion about that.

Q Let's finish up where we were with the invoices. So if you would put Exhibit 5, 6 and 7 back in front of you.

Q The first time you saw the report, how long was it?
A How long was the report?
MS. ALLEN: If you don't know, you don't have to speculate.
THE WITNESS: I don't recall.
BY MS. DE MORY:
Q Do you recall whether it was more than five pages the first time that you saw it?
A I don't remember.
Q The first time you saw it, were your opinions already set forth in the draft?
A I don't remember the exact, you know, timing of things, but the opinions were being entered into the report. And, of course, gradually, eventually they ended up in the report.
Q Prior to June 12th of 2006, had you physically looked at any of the Customer Defendant designs that are at issue in this litigation?
MS. ALLEN: Again, you don't have to speculate, but if you know, you can answer.
THE WITNESS: I did not.
BY MS. DE MORY:
Q When was the first time that you looked at a customer design that is at issue in this

generic.

Q So if we exclude reviewing the draft, did those 4 hours reflected on this July 3, 2006 invoice reflect the time during June that you spent reviewing documents that were produced by the parties in the litigation?

A That is correct.

Q I'm going to hand you what we will mark as, quite unfortunately, Exhibit 11. I say quite unfortunately because it's so big.

A Is this a single exhibit?

Q It is. Actually, she'll have to put a sticker on the front of it.

(Papaefthymiou Exhibit 11 identified.)

BY MS. DE MORY:

Q I will represent for the record that Exhibit 11 is comprised of all of the exhibits to your report. So rather than attaching that stack to every report, I've marked one exhibit, 11.

And for right now, I want to turn to appendix B, which is tabbed right up there, way up at the top just B. You've got it right up there, just the two pages.

A Yeah.

Q You see this list of other documents that

A No.
Q I'm going to hand you what I will mark as the next exhibit in order, which is 12.
(Papaefthymiou Exhibit 12 identified.)
BY MS. DE MORY:
Q Do you recognize Exhibit 12?
A No.
Q Do you know if you have seen Exhibit 12 before?
A I don't recall seeing it before.
Q Would you turn to page 15 of Exhibit 8? It's the one right there on top.
A 8, okay.
Q Last page.
A Okay.
Q With reference to Exhibit C, what do you recall seeing with regard to an HDL operator search report, or do you recall ever seeing an HDL operator search report?
A There was discussion about it in the conference calls, and I had -- I was told about certain numbers that came out of the searches with respect to key words and that's basically the extent.
Q So you didn't actually see these HDL

than one function. I'm not sure what that means.

BY MS. DE MORY:

Q Do you have an opinion whether or not the Customer Defendant designs are architecture independent if architecture is defined as the architecture of the entire circuit that is input into the tool?

MS. ALLEN: Objection; vague and ambiguous, compound.

THE WITNESS: I certainly have an opinion with regard to what the customer inputs, the Defendant inputs, make use of architecture independent operators, actions and conditions.

MS. ALLEN: Can we go off the record for a second?

MS. DE MORY: I'll give you a second to go ahead and do whatever you need to do.

MS. ALLEN: We can keep going. We can do this after. If you feel like you're not at a good stopping point, that's fine.

BY MS. DE MORY:

Q Do you agree that in the context of the customer designs, prior to the time that the RTL is written for the design, a -- the designer -- a designer actually makes decisions about where

various registers are going to be located in the design, the functions between registers and the cycle by cycle behavior of the circuit?

MS. ALLEN: Objection; compound, vague and ambiguous, calls for speculation and overly broad.

THE WITNESS: I have no way of knowing what the specific customers did before describing their designs in Verilog HDL.

BY MS. DE MORY:

Q Because you didn't read their depositions; right?

A Well, I didn't go through their depositions in detail, that's --

Q That's true?

A You could say that.

Q So it's not true that you have no way of knowing that; isn't that correct?

MS. ALLEN: Objection; vague and ambiguous and calls for speculation.

BY MS. DE MORY:

Q Can you answer that?

A Well, I can certainly -- I can certainly -- I can certainly inform myself about the things that are in the depositions, material which has been given to me.

from the scope of its claimed invention."

It goes on and says, "Ricoh responds that the patentee's use of the term, 'register-transfer level' was merely a shorthand reference to denote the 'structural' RTL-type, as opposed to 'functional' RTL-type, of input systems prevalent at the time."

Do you see that?

A Yes.

Q And if you move down to line 9 on page 12, the court says, "Furthermore, an examination of the '432 patent's public record fails to provide any support for Ricoh's distinction between 'structural' and 'functional' RTL-type input systems."

Do you see that?

A Yes.

Q Do you agree with that statement?

A It is what the court states.

Q You don't dispute it?

MS. ALLEN: Objection; outside the scope of the opinion.

THE WITNESS: I wasn't asked to look into the specific issue raised in the statement.

BY MS. DE MORY:

Q So did the statement, "Furthermore, an

intend to qualify in any way the statement, "The prosecution history indicates that the patentee expressly disclaimed all register-transfer level descriptions," then -- strike that. Let me start over.

If the Court did not intend to qualify the statement, "The prosecution history indicates that the patentee expressly disclaimed all register-transfer level descriptions," your expert report does not address that issue?

MS. ALLEN: Objection; compound and vague and ambiguous and incomplete hypothetical.

THE WITNESS: I cannot -- my opinion was based on the -- on what the claim construction was, and I haven't really considered what it could have been if the claim construction were different.

BY MS. DE MORY:

Q So if the claim construction is that the prosecution history indicates that the patentee expressly disclaimed all register-transfer level descriptions, you haven't offered an opinion on whether or not the Customer Defendant designs would meet that claim construction; is that correct?

MS. ALLEN: Objection; compound, vague and ambiguous, assumes facts not in evidence, incomplete

hypothetical.

THE WITNESS: It's a completely separate question.

BY MS. DE MORY:

Q Your opinion depends on the fact that the Court intended to qualify register-transfer level descriptions with "as taught in Darringer"?

A My opinion is based on the exact text that I see as the final say of what the Court construes as architecture independent actions and conditions, that is correct.

Q And your opinion is not based on the sentence, "The prosecution history indicates that the patentee expressly disclaimed all register-transfer level descriptions;" is that correct?

A As I said, I took the entire claim construction order into account as I was preparing my opinion. And at the end of the day, the statements that were basically -- that formed a basis of any opinion were exactly what you see at the end of that section between lines 16 and 19.

Obviously, the Court took into account all these other previous statements in formulating -- in construing the claims. I did too as I was going

through the claim construction order. At the end of the day, the terms are construed the way that we see in line 16 through 19, so that was the basis for the opinion.

Q So if there's anything prior to line 16 through 19 that's inconsistent or not exactly congruent with what's in line 16 through 19, you didn't -- that didn't form the basis for your opinion. Is that fair?

A It was taken into account, if there were such inconsistencies.

You did point out something which may be viewed as an inconsistency on line 15. But, again, there needs to be a basis, and that basis is what you see between 16 and 19, between line 16 and 19. That was the basis for the report.

Q So if the Court thinks that what is taught in Darringer is all register-transfer level transfer descriptions, then you haven't offered an opinion on whether or not the Customer Defendant inputs are architecture independent; is that correct?

MS. ALLEN: Objection; vague and ambiguous and assumes facts not in evidence, incomplete hypothetical.

THE WITNESS: I have offered an opinion

independently of the court construction about the nature of the inputs of the systems that the Darringer patent describes, and the nature of these inputs is structural. We discussed, as you asked me before, about the simple transformations, and how I inferred that the inputs of the Darringer are structural, and that is a separate -- that is a separate opinion.

BY MS. DE MORY:

Q And you don't think, as you sit here today, that the court has already rejected that opinion that the Darringer inputs are structural RTL; is that right?

A I have no -- I don't know what the court may or -- to my own -- I don't know.

Q Nothing in the paragraph prior to line 16 through 19 leads you to believe that the court has already rejected your opinion that the inputs to the Darringer system are structural RTL; is that correct?

MS. ALLEN: Objection; vague.

THE WITNESS: The way that I read the previous text, I do not draw this conclusion.

BY MS. DE MORY:

Q And you also -- strike that.

and compound.

THE WITNESS: That is a slightly different question, right, because having a description presented to the tool and requiring the tool to generate a design is one thing. The tool may still be able to handle the description in certain ways, simulate it, for example, and still be unable to generate the design.

So that's why I'm saying, one of the reasons that it's not clear to me exactly what is it that you require. You clarified, and we can leave it there.

BY MS. DE MORY:

Q The requirement -- the definition of "require" is that the input results in an output that is a valid portion of an ASIC or the entire design for an ASIC?

A Okay.

Q And so my question is, going back to the most general question, which is at any time, did Design Compiler require the input to specify a description of how the chip outputs and latches are set according to the value of the inputs for a clock cycle?

A The answer is I don't know.

Q And the answer is you don't know whether I ask you about 1997 or 2000 or 2003; is that correct?
A Correct.
MS. ALLEN: Objection; compound.
THE WITNESS: I don't know.
BY MS. DE MORY:
Q The answer is you don't know if I ask you about today; is that correct?
A Today, my understanding -- and I must say that I have not used Design Compiler myself recently. I do rely on the opinion that I set forth. I did rely and I do rely on Dr. Soderman, but my impression is that today Design Compiler can handle behavioral descriptions, and they wouldn't necessarily be descriptions that fit exactly the description that you gave, the narrow -- relatively narrow description that you gave.
BY MS. DE MORY:
Q When you said behavioral descriptions in your last answer, what did you mean?
A A description which says more about the intended function of a system as opposed to how this function is implemented as opposed to the structure of the system.
Q So -- and what did you mean in your last

outputs and latches are affected by the value of the inputs doesn't require -- strike that.

How does specifying how, for a single clock cycle, the chip outputs and latches are affected by the value of the inputs require specifying particular hardware components?

A It does not necessarily require it.

Q Do you agree that one generally understood definition of RTL includes the fact that the cycle by cycle behavior of the circuit is described in the input?

MS. ALLEN: Objection; vague.

THE WITNESS: At some point in time, that was probably the case.

BY MS. DE MORY:

Q Is that the case today?

A I don't think so.

Q Is describing the cycle by cycle behavior of the circuit something that is, to your knowledge, has it ever been a requirement of the input to Design Compiler?

A I don't know.

Q Turning to page 6 of your report, in the middle of the second full paragraph. And there is a sentence, and you can read the rest of the paragraph

Q Now, my question is -- and I also understand that you have not undertaken to determine whether or not the inputs to the designs are functional or structural RTL; is that correct?

A That is correct.

Q And, in fact, as part of your opinion, you have not undertaken to determine whether they are any kind of RTL. Your opinion is that they use architecture independent actions and conditions; is that correct?

A Correct, this is one of the opinions.

Q Do you know whether to determine whether or not something is structural, functional or some other kind of RTL, you need to look at more than a single operator in the design?

MS. ALLEN: Object as vague and ambiguous, and you guys were really quick on the last question and answer, but I want to interject misstates prior testimony.

THE WITNESS: So the question, once again, was whether I know --

BY MS. DE MORY:

Q Well, the question is not necessarily whether you know. Can you determine if something is structural or functional or RTL at all by looking at

one operator in a design?

MS. ALLEN: Objection; incomplete hypothetical, vague.

THE WITNESS: If you just give me one line without telling me where this line came from. I don't know what that line is.

BY MS. DE MORY:

Q So from just one line of code, you can't tell whether or not the input for a particular ASIC is functional RTL or structural RTL or RTL at all; is that fair?

MS. ALLEN: Objection; vague and incomplete hypothetical.

THE WITNESS: One line doesn't say anything, really, for the question that you asked.

BY MS. DE MORY:

Q To determine whether or not input code is RTL, do you need to know more than the types of operators that are included in the input?

MS. ALLEN: Vague.

THE WITNESS: Again, this is a line of questions that we had a few hours ago. It boils -- what is the meaning of RTL? What is the definition of RTL?

At the moment you gave me a description of

to algorithms.

Q And algorithms are a behavioral description; is that right?

A An algorithm is -- I wouldn't equate it to -- they're not the same thing.

Q It could be a behavioral description?

A It's the other way around, really. A behavioral description is an algorithm.

Q Okay. I'm going to hand you what we will mark as Exhibit 16.

(Papaefthymiou Exhibit 16 identified.)

BY MS. DE MORY:

Q The first question is, have you ever seen this entire file before, which is lpfiler.v?

(Pause.)

A Well, I must have seen it at some point because on page 10 of my report, I have a part of this file. So the name doesn't really ring too many bells, of course, but it's almost the same name. So, yeah, I've looked at all sorts of files. I wouldn't have a way to remember specific files.

Q And how did you look at these files? Were they paper?

A You know, I've looked at files like this, printouts sitting in front of a terminal. And

having the files electronically, you know, showing up in front of me, in front of the monitor, I've seen versions of electronic files in conference calls. So in all sorts of, you know, various ways.

Q Now, did you review the -- Ricoh's final infringement contentions?

A The name of the document sounds familiar. I may have been given a copy, but I don't really remember.

Q It's not something that you spent very much time looking at?

A I don't remember.

Q It's three binders of documents that are claim charts for each one of the ASICs. Do you recall seeing that?

A That doesn't -- I mean, your description doesn't really ring any bells.

Q Which means you probably didn't see it if it's comprised of multiple binders of claim charts?

A Probably.

MS. ALLEN: Objection; assumes facts.

BY MS. DE MORY:

Q Now, other than looking at the one portion of code that you pulled out of here, which is on page 5, actually, and there's a little part of it

CONFIDENTIAL:
SUBJECT TO PROTECTIVE ORDER

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UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INCORPORATED, et al., Defendants	**CASE NO. C-03-4669-MJJ (EMC)** **CASE NO. C-03-2289-MJJ (EMC)**
SYNOPSYS, INC., Plaintiff, vs. RICOH COMPANY, LTD., Defendant	**RICOH'S EXPERT REPORT OF MARIOS PAPAEFTHYMIOU ON INFRINGEMENT BY AMI SEMICONDUCTOR, INC.**

I. Introduction

In this litigation, Ricoh Company Ltd. ("Ricoh") has asserted that AMI Semiconductor, Inc. ("AMIS") infringes and has infringed claims 13-17 of U.S. Patent No. 4,922,432 (the "'432 Patent") by performing certain processes in the design and production of ASICs. The '432 patent is owned by Ricoh, and collectively, I refer to claims 13-17 of the '432 Patent as the "asserted Ricoh claims."

This report is directed to, and will focus on, the nature of the inputs that Ricoh asserts are part of the accused processes. In particular, this report sets forth my opinion, and the basis therefore, that AMIS has used input specifications comprising architecture independent actions and conditions in connection with the design and production of certain ASIC products that I have been informed are sold, offered for sale, and/or imported into or exported out of the United States. This report also sets forth my opinion that these architecture independent inputs are not the type of "Register-Transfer Language (RTL)" formatted input specifications taught by the Darringer Patent (U.S. Patent No. 4,703,435) that was considered by the Court during claim construction.

II. Retention

Ricoh has retained me as an expert witness in this litigation. I am being paid $250 per hour for non-testifying work, and $500 per hour for testifying work in this case. I have no personal interest in this litigation.

I am a Professor of Electrical Engineering and Computer Science at the University of Michigan. My research interests are in the areas of computer-aided design, and VLSI (including custom and ASIC design). I have taught senior and graduate-level courses in logic synthesis and VLSI design. My research and teaching activities routinely involve hardware description languages, commercial design tools by Synopsys and other vendors, ASIC designs, and ASIC design processes at all levels of abstraction.

Appendix A, attached hereto, includes my *curriculum vitae*. My *curriculum vitae* includes additional details regarding my qualifications for forming the opinions provided herein. Exhibit A also includes a list of my publications and a list of the cases in which I have testified at deposition, hearing or trial during the past four years.

The opinions provided in this report are based on my own personal knowledge and professional judgment. If called as a witness during trial in this matter, I am prepared to testify competently about them.

III. Preparation For This Report

In addition to studying the '432 patent, its file history, and the Court's April 7, 2005 claim construction order (the "Claim Construction Order"), I have reviewed the information cited herein, including the cited: documentation; depositions of the employees and designated representatives of the parties in this case; the Darringer Patent, its file history and references cited therein; the cited declarations submitted on behalf of the parties; and information from the documents listed at Appendix B, which is attached hereto.

This report is based on my study of the information available to me at the time of its writing. I reserve the right to update, supplement or amend this report in view of additional information obtained through discovery or other information that is now or might become available between now and trial that is significant to the opinions set forth herein.

IV. Complete Statement Of Opinions

A. Technology Background

The asserted claims of the '432 patent are directed to a process for designing ASICs. ASICs are integrated circuit chips designed to perform a specific function. ASICs comprise interconnections of transistors that receive input data signals and produce corresponding output data signals. Typically, the operation of these transistors is controlled by one or more controllers which cause data values to be stored in memory (e.g., Random Access Memory ("RAM") or

Read Only Memory ("ROM")), and a clock is used to trigger the storing of data values. Specific configurations of transistors are often grouped together to form logic operations. For example, an AND logic operation represents a configuration of transistors that produces a specific output Z = X AND Y for a certain configuration of inputs X and Y in accordance with the following truth table:

Z = X AND Y		
X	Y	Z
0	0	0
0	1	0
1	0	0
1	1	1

Similarly, OR, NOT, NAND, and NOR[1] logic operations each represents a configuration of transistors that produce a specific output for a given input.

Z = X OR Y			Z = NOT X	
X	Y	Z	X	Z
0	0	0	0	1
0	1	1		
1	0	1	1	0
1	1	1		

[1] The NAND function is equivalent to the NOT AND function, and the NOR function is equivalent to the NOT OR function.

Z = X NAND Y			Z = X NOR Y		
X	Y	Z	X	Y	Z
0	0	1	0	0	1
0	1	1	0	1	0
1	0	1	1	0	0
1	1	0	1	1	0

The logic operations are physically realized as hardware components of varying degrees of complexity. When ASICs are designed using logic synthesis, CAD tools are used to generate descriptions of the hardware components (and their interconnections); these descriptions are commonly known as netlists. The hardware components listed in the netlist are used to perform logic level operations of the ASIC. The netlist is targeted to a particular foundry process and in this sense is technology specific.

ASICs are designed using descriptions or specifications that describe the intended operations of the ASICs. These specifications can be input to CAD tools that perform logic synthesis to generate technology specific netlists for fabricating ASICs. The specifications that are input to such CAD tools can be written at various levels of abstraction. At higher levels of abstraction, the specification is easier to write and to understand, but harder to synthesize into a description that can be used to fabricate an ASIC. As CAD tools for logic synthesis evolved over time, so did their ability to synthesize inputs described at increasingly higher levels of abstraction.

Prior to the proliferation of CAD tools for ASIC design, many integrated circuits were designed manually, and required designers to describe the circuit operation at a low level, such as at the transistor level. Manually designing integrated circuits was time consuming and

error prone and became impractical as market demands led to more and more functions being incorporated into circuit operations.

CAD tools evolved to accept graphical descriptions (known as "schematics") of integrated circuit hardware components. At that time, CAD tools commonly were capable of converting the schematics to netlists that could be used for fabricating the ASICs. Although such CAD tools required less design time than completely manual processes, the step of creating schematic input descriptions was very time consuming and required detailed knowledge of the hardware architecture of the ASIC components.

CAD systems further evolved to accept textual descriptions of the operation of ASICs. These textual descriptions expressed ASIC operations in terms of Boolean operations that describe the logic level operation of an ASIC in a short hand format. These logic-level Boolean descriptions often were technology independent representations of ASICs in terms of AND/OR/NOT, and NAND/NOR logic operations. For example, the statement A • B meant A (AND) B and represented a logic level AND operation like that described at page 4 supra; and the statement A + B meant A (OR) B and represented a logic level OR operation like that described at page 4 supra. Such descriptions could be input to CAD systems which would ultimately map the minimized description to technology dependent hardware cells targeted to the selected foundry's process. Such descriptions were at a higher level of abstraction than the transistor level and schematic input descriptions that preceded them. Designing ASICs using these logic level and Boolean descriptions, however, was still time consuming and required a high level of skill and understanding of the logic operations that comprised the ASIC hardware architecture.

Over time, CAD tools have evolved to accept input formats in hardware description languages (HDLs) that described the function, behavior or operation of the ASIC to be designed

without needing to describe the underlying hardware architectures for performing the desired function, behavior or operation. These functional or behavioral HDLs describe the design in terms of higher level functions to be performed. Such higher level descriptions do not require detailed knowledge of the ASIC hardware architecture or implementing technology. For example, such descriptions do not require knowledge of the logic level operations implemented by the hardware components that can be selected for inclusion in the netlist. As such, ASIC designers often use functional or behavioral HDL descriptions to describe complex operations such as arithmetic operations (e.g., addition, multiplication) and conditional statements (e.g., IF and CASE statements). These functional or behavioral descriptions are also used to synthesize memory devices, finite state machines, as well as operations that cannot be performed in a single clock cycle ("multi-cycle" operations). Today, these higher level functions are commonly written in one of two HDLs known as Verilog and VHDL.

The term "RTL" or "register transfer language" has been used at times to describe HDL inputs to logic synthesis tools (including synthesizable Verilog and VHDL). The use of the term "RTL" has varied over time, however, and is now primarily dependent on the context. Many types of RTL exist and have been used to describe ASICs for purposes of logic synthesis. In the mid-1980s, structural RTLs that comprised technology independent representations of ASICs in terms of logic operations such as AND/OR/NOT, and NAND/NORs were commonplace. By the early 1990s, functional RTL formats, including functional descriptions written in Verilog and VHDL languages started becoming more prevalent than architecture dependent descriptions such as structural RTLs for describing many portions of ASICs being designed. Today, ASIC input descriptions having a range of abstraction levels are written in VHDL and Verilog formats. For example, higher level functional or behavioral input

descriptions as well as lower logic-level or Boolean descriptions can be written in Verilog or VHDL for input to Synopsys Design Compiler System[2] logic synthesis tools.

B. Statement Of Opinion

It is my opinion that as part of performing the processes alleged to infringe the asserted Ricoh claims, AMIS inputs architecture independent descriptions to a logic synthesis tool known as the Design Compiler System. These architecture independent descriptions are functional or behavioral descriptions that do not imply a set architecture, structure or implementing technology. It is also my opinion that these architecture independent input descriptions are not the RTL descriptions taught by Darringer.

1. Relevant Claim Language And The Court's Construction

The '432 patent claims architecture independent input descriptions. Specifically, claim 13 of the '432 patent recites the step of "...describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions...." It is my understanding that the Court has construed this claim language to mean "describing an input specification containing a series of desired functions to be performed by the desired ASIC." (Cl. Construction at 14). It is also my understanding that the court has construed the term "architecture independent actions and conditions" to mean the "functional or behavioral aspects of a portion of a circuit (or circuit segment) that does not imply a set architecture, structure or

[2] As used herein the term "Design Compiler System" includes: 1) a software product provided by Synopsys, Inc. ("Synopsys") known as "VHDL Compiler" or "HDL Compiler for Verilog" (generically referred to herein as "HDL Compiler"); 2) a software product provided by Synopsys known as "Design Compiler" (including Design Compiler (or DC), DC Ultra, DC Ultra Opt, DC Expert, DC Expert Plus and DC Pro); and 3) certain Synthesis Libraries. As used herein the term "Synthesis Libraries" includes: synthetic libraries provided by Synopsys known as "standard.sldb, dw_foundation.sldb, dw01.sldb, dw02.sldb, dw03.sldb, dw04.sldb, dw05.sldb, dw06.sldb, dw07.sldb, and dw08.sldb" (hereinafter "the DesignWare synthetic libraries"); and physical libraries provided by one or more foundries (hereinafter "Technology Libraries").

implementing technology, but excludes the use of register-transfer level descriptions as taught in Darringer" (Cl. Construction at 12).

2. The Accused Processes Use Architecture Independent Inputs

Having reviewed HDL inputs used by AMIS in this litigation, it is my opinion that AMIS uses input specifications that include high level, functional or behavioral ("architecture independent") inputs to perform processes that infringe claims 13-17 of the '432 patent. In particular, AMIS uses HDL (i.e., Verilog and VHDL) input specifications that contain descriptions of functionality or behavior desired in the ASIC product under design without expressly (or implicitly) describing the architecture, structure, or implementing technology needed to perform such functionality or behavior.[3] The input specifications used by AMIS in this litigation thus meet the definition of "architecture independent actions and conditions," as that term is construed by the Court in its Claim Construction Order. Examples of AMIS descriptions include those set forth below:

[3] It is my understanding that AMIS has stated in declarations and deposition testimony in this case that it uses Verilog and VHDL input specification formats for synthesis of ASICs using Design Compiler. (See, e.g., Supplemental Input Declaration Of Robert B. Smith Of AMI dated January 12, 2006; Clifford Warren 6/8/2006 Deposition Tr. at 26-30, 53-54; Robert Smith 2/9/2006 Deposition Tr. at 89, 110, 2/10/2006 Deposition Tr. at 206-219). I have also reviewed ASIC design specifications including functional or behavioral descriptions produced by AMIS in this litigation, some of which were written in Verilog and others in VHDL; examples of these functional or behavioral inputs are included in Appendix C, attached hereto.

Arithmetic operations such as addition (commonly denoted by "+") and multiplication (commonly denoted by "*"). An example input segment code is set forth below. Many similar inputs can be found throughout the input descriptions of the accused AMIS products.[4]

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"If" statements, "If-Then" Statements, "If-Then-Else" Statements. An example input segment code is set forth below. Many similar inputs can be found throughout the input descriptions of the accused Aeroflex products.

[4] As used in these examples, the "+" represents an arithmetic addition operation, not a logical OR function.

CONFIDENTIAL:
SUBJECT TO PROTECTIVE ORDER

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The above examples are functional or behavioral descriptions that do not imply a set architecture, structure or implementing technology. AMIS uses many functional and behavioral inputs including arithmetic operators (e.g., +, -, * /), relational operators (e.g., <, >, <=, >=), "if" statements, "case" statements, "wait" statements, "always" statements, etc. and other high-level functional descriptions (e.g., finite state machines). Additional examples of such inputs are set forth in Appendix C.

a. The Darringer Patent Teaches Architecture Dependent RTL

i. The Darringer Patent Does Not Teach The Inputs Claimed In The Asserted Claims Of The '432 Patent

It is my understanding that the Court in this case has construed the claimed inputs to exclude the use of RTL descriptions as taught in the Darringer Patent. In my opinion, the Darringer Patent uses the term "RTL" in the sense of the older (then-prevalent) structural RTL that is not claimed by the '432 patent. As noted above at page 7 supra, the RTL commonplace at the time of the Darringer Patent (i.e., in the mid-1980s) was a form of structural, architecture dependent input that included short hand representations of desired logic operations (e.g., AND/ORs and NAND/NORs, etc.) of the ASIC[5] and a flowchart-like specification of control that described how chip outputs and memory elements (i.e., latches) were set on each clock cycle. (Darringer Patent, col. 5 lines 27-38). That the RTL used in the Darringer Patent closely describes the architecture of the hardware desired in the design is evident from the requirement

[5] The difference between the inputs disclosed in the Darringer Patent and claimed in the '432 patent was recognized during prosecution of the '432 patent when the patent applicant argued that the "specifications used by Darringer et al. are not truly at an architecture independent level, but rather are at a lower level which is indeed hardware architecture dependent and defines the system at a 'register-transfer' level description." (See Cl. Construction at 11 quoting '432 Patent Pros. History at Nov. 1988 Amendment p. 7 (emphasis in original)).

in the Darringer Patent that the inputs undergo a simple translation of the specification into equivalent AND/OR logic. (Darringer Patent, col. 5 lines 35-41) ("At step 102 in FIG. 2, the register-transfer level description undergoes a simple translation to an initial implementation of AND/OR logic. This AND/OR level is produced by merely replacing specification language constructs with their equivalent AND/OR implementations in a well known manner.").

Like the Boolean descriptions noted above at pages 4-6, supra, the use in the Darringer Patent of descriptions that are simply translated (by merely replacing specification language constructs with logic operations) is, in my opinion, a description that either expressly specifies (or at least implies) a set architecture or structure desired to be used in the ASIC under design. Specifically, the Darringer Patent teaches logic level inputs that specify or imply a set architecture of AND/OR logic operations. As noted above at page 7, supra, such descriptions were well-known and commonplace for use in logic synthesis at the time of the Darringer Patent (i.e., in the mid to late 1980s). In my opinion, Darringer is not directed and does not teach logic synthesis processes using high level, functional or behavioral input descriptions such as the architecture independent input descriptions of the '432 patent.

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ii. Darringer Does Not Teach The Inputs That Are Part Of the Accused Processes

The Darringer Patent does not teach the inputs that Ricoh asserts are used as part of the accused AMIS processes. The Darringer Patent discloses that the system has only limited capability for synthesizing inputs. Specifically, the Darringer Patent states the inputs undergo "a simple translation to an initial implementation of AND/OR logic."

The accused AMIS inputs do not specify or imply set logic level descriptions such as AND/OR logic operations as taught by Darringer. Unlike the Darringer Patent inputs, the inputs that are part of the accused AMIS processes are not architecture dependent and do not undergo a "simple translation" to an initial implementation of logic-level (e.g., AND/OR) representations by "merely replacing specification language constructs with their equivalent AND/OR implementations," as required in the Darringer Patent. Rather, AMIS uses the Design Compiler System to synthesize architecture independent Verilog and VHDL descriptions of the functional or behavioral aspects of a portion of an ASIC or ASIC segment.

It is my understanding from my conversations with Dr. Soderman that the accused processes use architecture independent descriptions that undergo a complex mapping process

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using the Design Compiler System. In particular, the accused processes perform mappings using the architecture independent descriptions and generic operators[8] in order to select corresponding architecture dependent implementations, and ultimately technology specific hardware components used in the ASIC under design. Such a process is not used (and, indeed, not needed) in the Darringer Patent.

V. Conclusion

In my opinion, AMIS uses input descriptions that are not disclosed in the Darringer Patent. Unlike the Darringer inputs, the AMIS inputs are architecture independent descriptions that describe function or behavior and do not imply a set architecture, structure or implementing technology and that do not undergo a simple translation to AND/OR logic operations.

VI. Appendices

A. *Curriculum Vitae* Of Marios Papaefthyimiou
B. List Of Materials Reviewed In Developing Opinions
C. HDL Operator Search Report (CD Bates No. RCL000011956)

Executed on June 23, 2006

/s/
Marios Papaefthymiou, PhD

[8] Generic operators include synthetic operators (e.g., ADD_UNS_OP) and other operators such as MUX_OP, SELECT_OP, DP_OP, SEQGEN, FFGEN, and LOGDB.

IN THE UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

v.

AEROFLEX ET AL.,

Defendants.

Case No. C-03-4669-MJJ (EMC)

SYNOPSYS, INC.,

Plaintiff,

v.

RICOH COMPANY, LTD.,

Defendant.

Case No. C-03-2289-MJJ (EMC)

CERTIFICATE OF SERVICE

I am employed in Washington, District of Columbia. I am over the age of eighteen (18) years and not a party to the within action; my business address is 2101 L Street, NW, Washington, DC, 20037. On June 23, 2006, I served **RICOH'S EXPERT REPORT OF MARIOS PAPAEFTHYMIOU ON INFRINGEMENT BY AMI SEMICONDUCTOR, INC.** on the parties, through their attorneys of record, by sending true copies thereof to the e-mail addresses listed below:

Terry Corbin, Esq.
CorbinT@Howrey.com

Jacky Fink, Esq.
FinkJ@Howrey.com

Denise De Mory, Esq.
DeMoryD@Howrey.com

I declare that I am employed in the office of a member *pro hac vice* of the Bar of this Court at whose direction this service was made.

I declare under penalty of perjury that the foregoing is true and correct. Executed in Washington, D.C. on June 23, 2006.

Solomon Seyoum

APPENDIX B

- The Court's Claim Construction
- Other Documents
  - SP000071009-1100
  - RCL 000000001-0265
  - AF 000023286-3481
  - MGI 000033893-3908
  - MGI 00034098-4128
  - MGI 000034441-4448
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  - AMI 000000712-1206
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  - MES 000003264-3287
  - MGI 000009804-10414
  - AF 000042696-3124
  - SP 000095701-6322
  - RCL 000011420-1425
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  - SP 000168657-8785
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  - SP 000147523-7532
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  - RCL 000009449-9622
  - SP 000184344-4349
  - SP 000121644-1745
  - DEF 000027028-7054
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  - SP 000059888-60461
  - SP 000058826-8846
  - RCL 000007749-7753
  - RCL 000009658-9659
  - AMI 000021867-1939
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- SP 000098068-8593
- SP000002771-830
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- Darringer Patent File History & Associated References (attached to this AppendixB as Exh. 1)

- Depo Transcripts:
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  - Chiappini 2/23/2006, 2/24/2006, 6/7/2006
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  - Adams 12/21/2005
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  - Webster 6/8/2006
  - Zepter 12/22/2005
  - Coco 1/19/2006, 4/20/2006